Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) An EEPROM integrated circuit structure, the structure comprising:

a substrate including a surface region, the surface region being provided within a first cell region;

a gate dielectric layer of first thickness overlying the surface region of the substrate;

a select gate overlying a first portion of the gate dielectric layer;

a floating gate overlying a second portion of the gate dielectric layer and coupled to the select gate;

an insulating layer overlying the floating gate;

a control gate overlying the insulating layer and coupled to the floating gate; and

a tunnel window provided in a stripe configuration, the stripe configuration is disposed within a portion of the gate dielectric layer, the portion of the gate dielectric layer being of a second thickness, the second thickness being less than the first thickness;

wherein the stripe configuration extending across an entire length of the first cell region from a first field isolation oxide region to a second field isolation oxide region;

wherein the stripe configuration extending through the first cell region as well as N other cell regions, N being greater than 2.

2. (Original) The structure of claim 1 wherein the gate dielectric layer comprises a silicon dioxide.

3. (Original) The structure of claim 1 wherein the tunnel window is characterized by a width of less than 0.25 microns.

4. (Original) The structure of claim 1 wherein the insulating layer is an ONO layer coupled between the floating gate and the control gate.

5. (Previously Presented) The structure of claim 1 wherein the floating gate has a width of 1.5 microns.

6. (Original) The structure of claim 1 wherein the tunnel window is provided using a phase shift mask.

7. (Original) The structure of claim 1 wherein the stripe configuration extends through a plurality of cells, each of the cells being separated by a field oxide region.

8. (Original) The structure of claim 1 wherein the substrate is a semiconductor wafer.

9. (Previously Presented) The structure of claim 1 wherein the select gate, floating gate, and control gate are provided within the first cell region, the first cell region being provided within an isolation region.

10. (Canceled)

11. (Previously Presented) A method for manufacturing an EEPROM integrated circuit structure, the method comprising:

providing a substrate including a surface region, the surface region being provided within a first cell region;

forming a gate dielectric layer of a first thickness overlying the surface region of the substrate;

patterning the gate dielectric layer to form a plurality of stripes, each of the plurality of stripes being characterized by a second thickness, the second thickness being less than the first thickness, each of the plurality of stripes having a predetermined width and a predetermined length, at least one of the plurality of stripes includes a stripe portion traversing through a portion of the first cell region and other cell regions;

forming a floating gate overlying a portion of the gate dielectric layer, the portion of the gate dielectric layer including the stripe portion traversing through the portion of the gate dielectric layer;

forming an insulating layer overlying the floating gate; and

forming a control gate overlying the insulating layer and coupled to the floating gate,

wherein the stripe portion-traversing across an entire length of the first cell region from a first field isolation oxide region to a second field isolation oxide region, the stripe portion includes a tunnel window for a memory device.

12. (Previously Presented) The method of claim 11 wherein the gate dielectric layer comprises a silicon dioxide.

13. (Original) The method of claim 11 wherein the tunnel window is characterized by a width of less than 0.25 microns.

14. (Original) The method of claim 11 wherein the insulating layer is an ONO layer coupled between the floating gate and the control gate.

15. (Previously Presented) The method of claim 11 wherein the floating gate has a width of 1.5 microns.

16. (Original) The method of claim 11 wherein the tunnel window is provided using a phase shift mask.

17. (Previously Presented) The method of claim 11 wherein the at least one of the plurality of stripes extends through a plurality of cells, each of the cells being separated by a field oxide region.

18. (Original) The method of claim 11 wherein the substrate is a semiconductor wafer.

19. (Previously Presented) The method of claim 11 wherein the floating gate and the control gate are provided within the first cell region, the first cell region being provided within an isolation region.

20. (Previously Presented) The method of claim 11 wherein at least one of the plurality of stripes runs through the first cell region to the other cell regions, the other cell regions being numbered from 2 through N, where N is an integer greater than 2.